Web Streamed SDR's in Service at GB2RHQ – Hack Green Bunker

Gateway to the Net .
We are fortunate to have a very fast internet service into Hack Green via a 5Ghz microwave link. The service provides a bandwidth of 50Mb/s in both upload and download directions. This capacity is then dynamically split between two IP addresses, one being used for bunker management, the other for GB2RHQ services.

The six publicly accessible SDR receivers are connected to a blade server running the 'Linux-Mint 16'operating system and the WebSdr software (see credits).
Each SDR is connected to the server via a high quality soundcard which in essence acts as an A/D converter. The bandwidth of the SDR receiver (bandwidth as seen on the PC screen) is determined by the sampling rate of its associated sound card. A sound card sampling at 192kHz will give a visible radio bandwidth of 192kHz (+/-96kHz) about the centre operating point.

Mint, as with all linux operating systems is a little "Geeky" to use, and being Windows orientated, quite frustrating (in my opinion) to learn. This is exacerbated by the sheer volume of incorrect and outdated Linux information found on the world wide web. Perhaps here is the best place in this article to point out that the Hack Green SDR project is very much a team effort, and I left most if not all of the programming tasks to Tony G1HMO and Martin G7CKX (see credits).

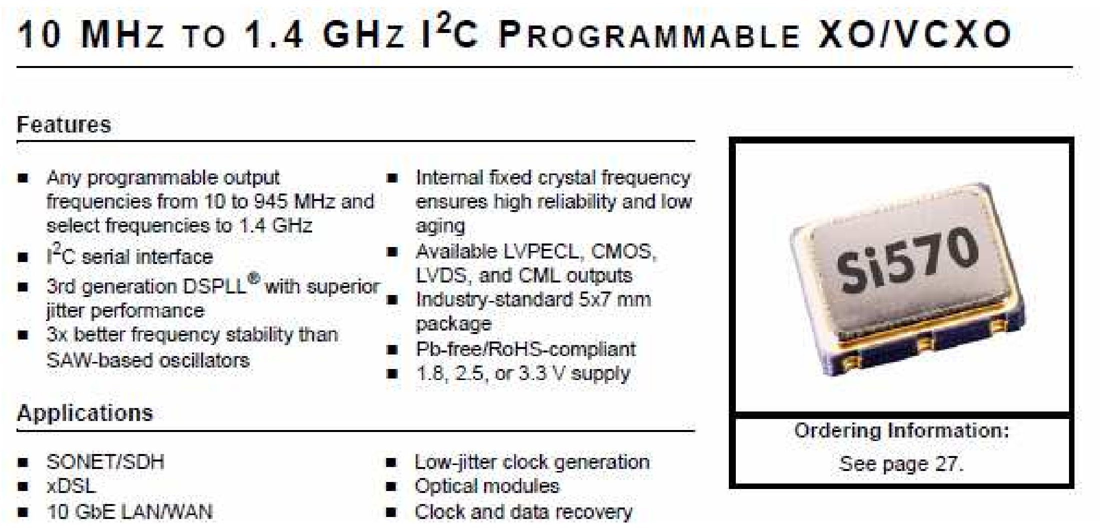
We started out with a well known SDR receiver which employed a crystal oscillator to define its centre frequency of operation. This set up allowed us to get the bugs out of the Mint system and sound drivers, and to begin to climb the learning curve discovering the many foibles of linux.

SDR design.

The noise floor of the "end to end" encoder system has two main component parts which contribute to the noise performance, the receiver's commutating detector and associated output amplifier plus the noise floor and performance of the sound card employed to encode the receiver output.
Under measurement we found the Finningly SDR had the edge on s/n+n and noise floor compared with other receivers. The main contributing factor for this was that the output amplifier of the Finningly SDR was designed to run from 12v DC rather than the regulated 5vDC sometimes employed by other receivers. Having a higher "aim" voltage quite often results in better dynamic range and linearity.

Getting the required operating centre frequency without the expense of crystal manufacture was one of our prime design aims, and we agreed with the designers of the Finningley SDR (see credits) that we could adopt the best aspects of their design and add features of our own.

The new design soon took on a quite different appearance once our “wish list” had been put down on paper, principally the use of aSi570 programmable oscillator, a microprocessor controller, plus a plug in front end filter to allow one pcb design to be used for many different bands.



10 MHz to 1.4 GHz I^{2}C Programmable XO/VCXO

Features

- Any programmable output frequencies from 10 to 945 MHz and select frequencies to 1.4 GHz
- I^{2}C serial interface
- 3rd generation DSPLL® with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Internal fixed crystal frequency ensures high reliability and low aging
- Available LVPECL, CMOS, LVDS, and CML outputs
- Industry-standard 5x7 mm package
- Pb-free/RoHS-compliant
- 1.8, 2.5, or 3.3 V supply

Applications

- SONET/SDH
- xDSL
- 10 GbE LAN/WAN
- Low-jitter clock generation
- Optical modules
- Clock and data recovery

Si570

Ordering Information:
See page 27.

The microcontroller software was written to provide multiple tasks and services including RS232 serial communication with the outside world, plus communication with the Si570. The internal tasks include programming the Si570 from a pre-stored frequency list, determined by the BCD value set on an i/o port on the PIC microprocessor using a bcd rotary switch.

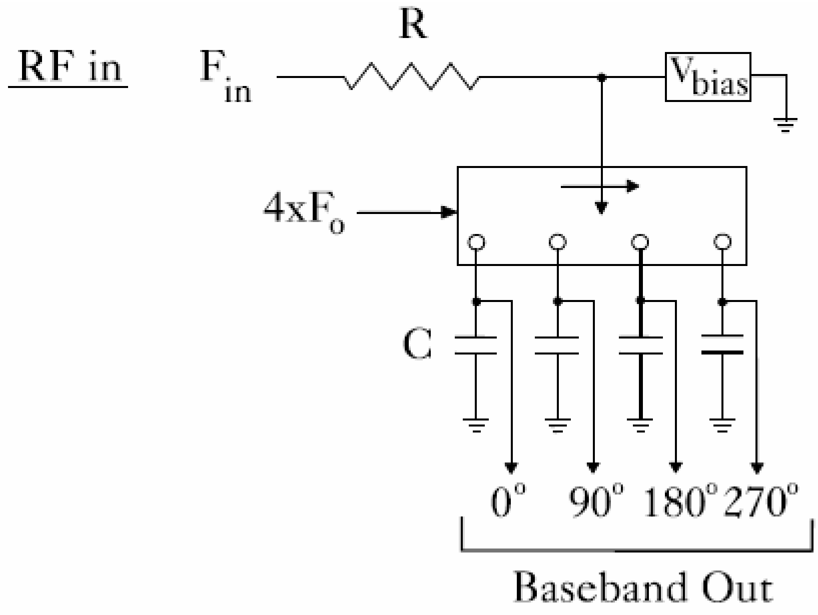
The external services permit the reading and writing of the Si570 internal frequency adjusting registers directly from the PC using RS232. This procedure is used as part of a calibration routine required once during the initial testing of the pcb. Additionally, a software routine was added which allowed a connected RS232 terminal or PC to increment / decrement the Si570 registers to give a “directly applied free tune” effect upon the SDR, and although fully functional, this feature is not yet used in our current web based setup.

A Visual Basic program was then written to allow easier access to and configuration of the Si570 registers making the job of initial calibration much less tedious than it would by using traditional methods.

By setting each receiver’s frequency of operation as the default (BCD zero) channel, the BCD switch can be left disconnected, thus the receiver adopts the desired band of operation automatically at power up.

The expensive parts of the system are the Si570 chips at £15 each, sound cards at around £50 each second user, and of course the server at £550 second user. Add to this list, electricity consumption at £450 PA, Aerial construction and passive splitting unit, public liability insurance as the aerial crosses a public space at 60 feet above ground.

Commutating Detector.
There is loads of information on the net for this type of detector and so I will just mention here it is a quadrature detector clocked at four times the desired centre frequency of the receiver and producing an “I & Q” output which is further processed by the PC sound card. This type of detector was around a long time before Dan Tayloe, but it may be true to say Dan first recognised the merits of this detector in SDR?



To quote Dan Tayloe, less than 1db conversion loss
Tracking bandpass Qs >3500 at 7Mhz

High 3rd order intercept point (+30dbm)

The detectors upper frequency limit is governed only by the ability of the chosen switch device (FET) to handle the switching times in a clean no jitter fashion, and can extend to 10Ghz using the latest devices, although above HF attention needs to be paid to the PCB layout and tracking.

Taking a look at the schematic for the Bunker SDR, top left of the schematic is the microprocessor and its associated Flash programming port J1. The programming interface to the Si570 oscillator module is “clock and data” at 3v3 logic level directly compatible with the chosen PIC16F688.

RS232 communications to the PIC are via J6, Q1, Q2 act as level converters translating the RS232 to 3v3 logic level and visa versa.

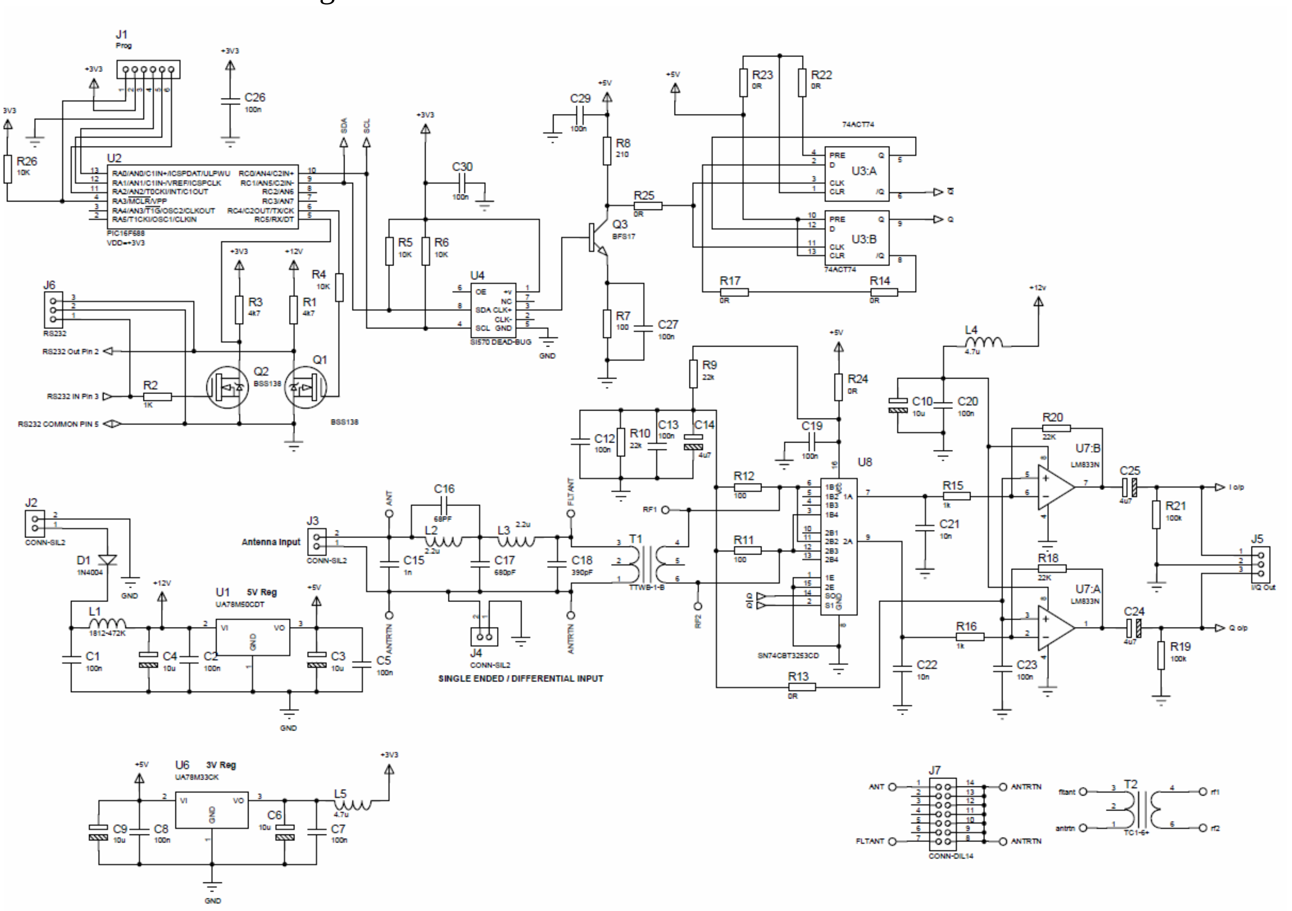
Output from the Si570 (3v3) is applied to Q3 level converter which in turn drives the 74ACT74 dual D type flip flop which outputs a Q and /Q (not Q) clock used to drive the SN743253 dual channel FET multiplexer used here as a commutating detector.
Note the DC bias applied by R11 & R12 on each channel input of the mux switch.

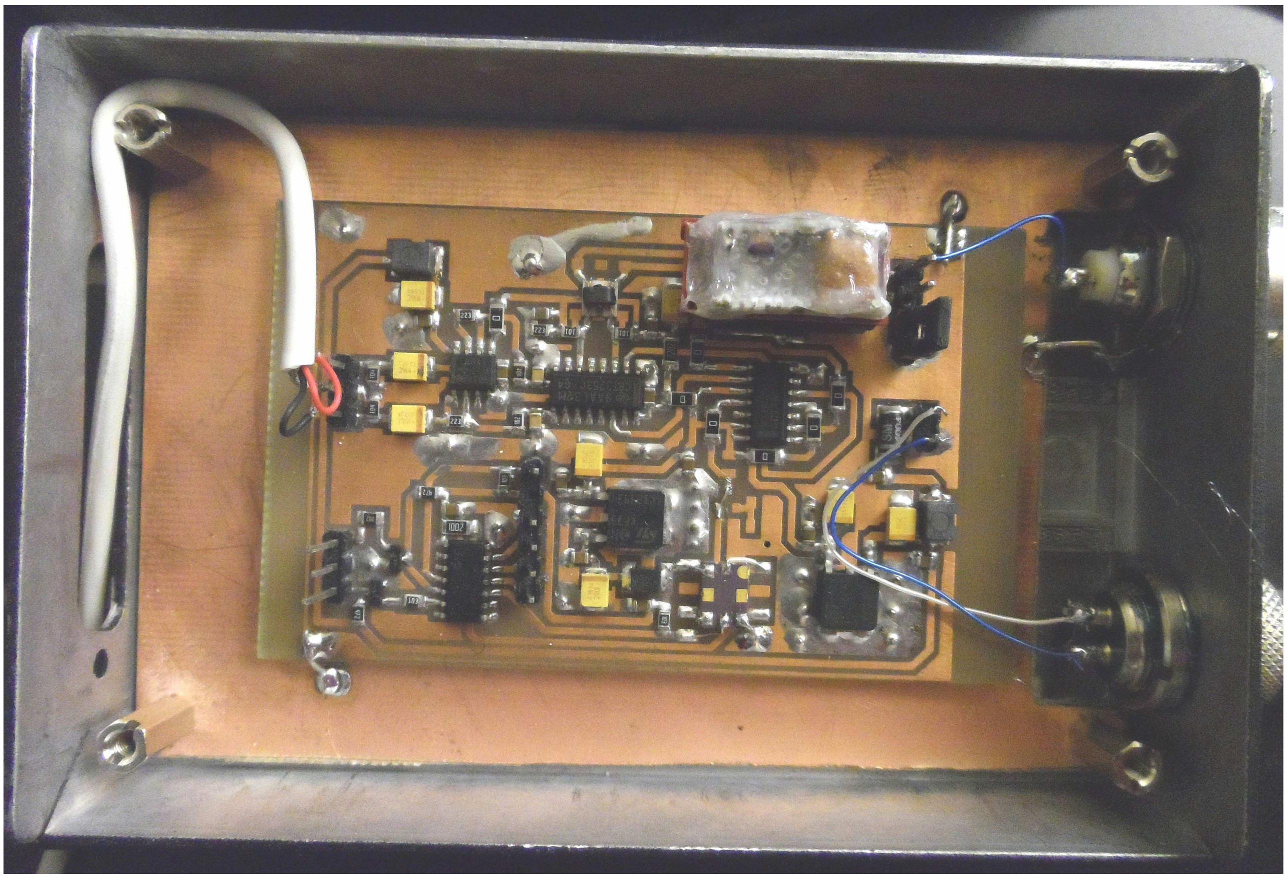
The RF input (J3) to the commutating detector is filtered by a simple LC arrangement which is realised in the hardware as SMT components mounted on a 14pin DIL carrier to facilitate easy changing of the working band.

The output of the commutating detector (I&Q) is filtered and amplified by U7 which as previously stated is run from the 12v DC input to give better dynamic range and noise performance.

The 5v and 3v3 regulated supplies are achieved by U1 and U6 respectively. In line with good pcb design, the 0v is distributed to all components via a ground plane covering the whole board. The design also avoided running “clock” lines under analogue circuits.

Bunker SDR Circuit Diagram





Internal view of one of the receivers.

The band filter can be seen top right (epoxy block) plugged in via a 14pin DIL connector. The PIC microprocessor is bottom left adjacent to the three pin header (RS232) and 5 pin header (flash programming port). Moving right, the 3v3 regulator, Si570 and 5v regulator on the bottom far right.

Above the Si570 is the dual D type flip flop, to the left of which is the dual mux (Commutating) detector and finally the dual operational amplifier for filtering and output of I&Q on the three pin header.

You will note the Si570 is mounted dead bug style and wired onto pads of the PCB. I decided that as this chip had 8 pads located on all sides, it would be a bit of a devil to get off the PCB should the need arise, but not a problem with the adopted mounting method.

On Test.
The minimum discernable signal under test conditions is 0,7uV PD CW and 1.8uv AM modulated 30%, as measured on an HP 8920A test set.

Future developments
The limiting factor with SDR is the cost and capabilities of the encoding sound card. Bandwidths which exceed the 192Khz sampling rate of the soundcard have to be sliced into what the user sees as the useful proportion of the band in question. It would be nice to be able to encode large segments of the spectrum for internet distribution, but the integrated circuits capable of doing this are expensive at this time.

At the time of writing the DONATE button on the sdr website has provided sufficient funds for electricity for 2014 operation, plus the purchase of some aerial components and an additional 2 sound cards, and the building of an aerial distribution unit.

The donate button will return to the site in October to raise funds for 2015 operation

Java
Java was the main source of complaint, but having implemented HTML5 on the 20th July 14 , has made Java problems a thing of the past, plus the SDR can now be accessed from mobile devices using Ios and Android.

Pieter-Tjerk Boer is thanked here for the free issue of his websdr software His website provides some interesting reading for the sdr enthusiast.
http://wwwhome.cs.utwente.nl/~ptdeboer/ham/sdr/

Credits :

Pieter-Tjerk de Boer (PA3FWM) Writer of the WebSDR software
Bernie Wright (G4HJW) Finningley designer
Kevin Avery (G3AAF) Finningley designer
Tony Steele G1HMO Software developer
Martin Steele G7CKX Hardware developer
Joe Bell G4PMY Test and calibration